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(54) PIXEL CIRCUIT, METHOD OF DRIVING THE SAME, AND ELECTRONIC APPARATUS

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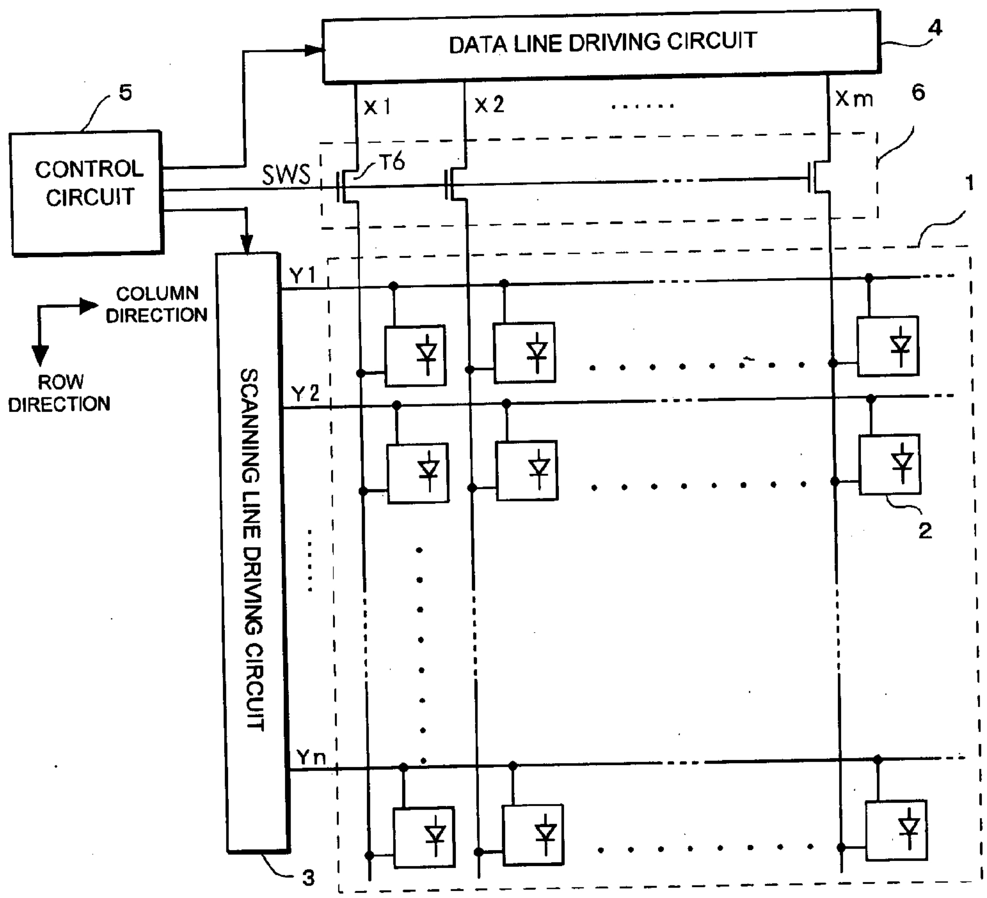
(57) **ABSTRACT**

To control variation in a driving current depending on Vth in a current program mode pixel circuit. In a state in which a variable current source **4**_a_ and a transistor **T3** are electrically isolated from each other, a gate voltage of the diode-connected transistor **T3** is set to an offset voltage (Vdd−Vth) according to a threshold voltage Vth thereof. Next, in a state in which the variable current source **4**_a_ and the transistor **T3** are electrically connected to each other, data based on the offset voltage and according to a product of a data current Idata and a supply time thereof are written in a capacitor **C1** connected to a gate of the transistor **T3**. And then, a driving current according to data stored in the capacitor **C1** is generated by means of the transistor **T3**, whereby brightness of an organic EL element OLED is set.



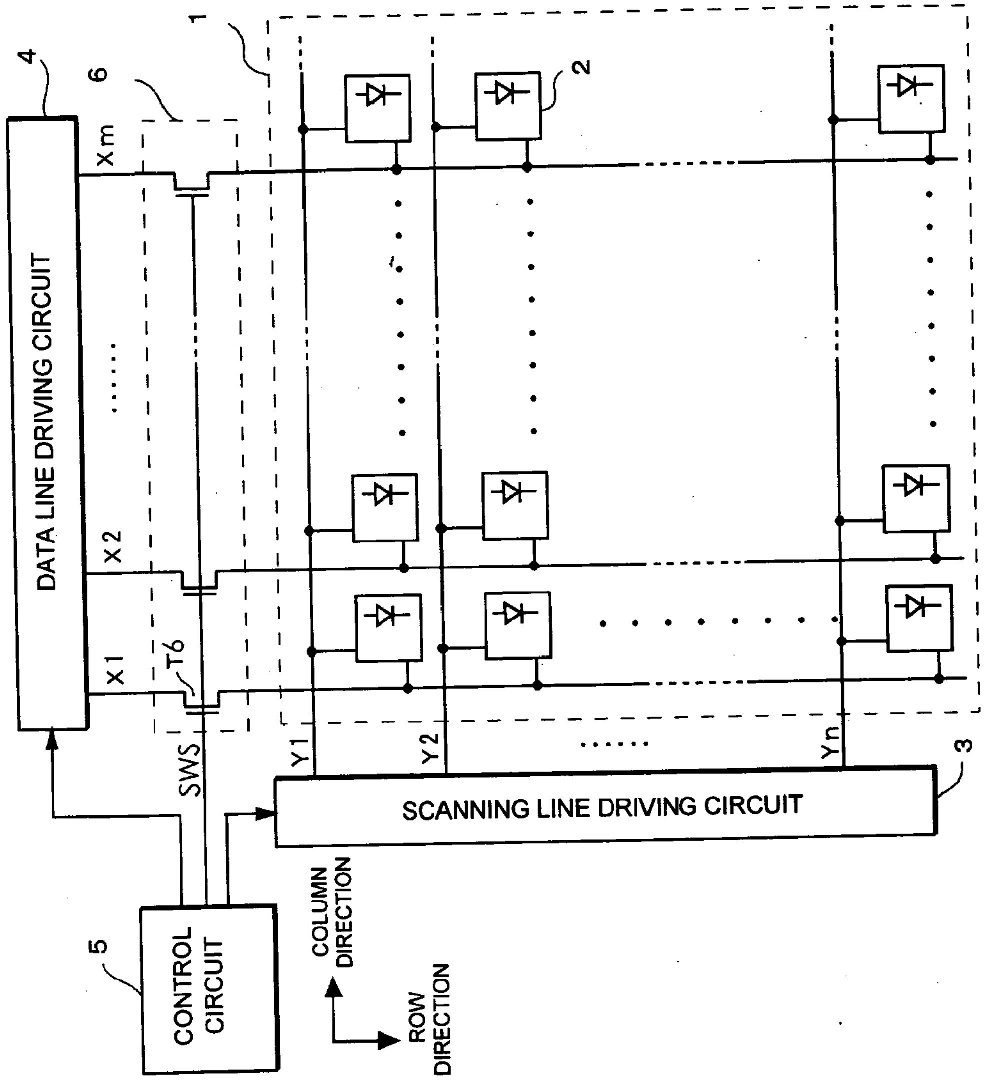

DATA LINE DRIVING CIRCUIT
4
6
1
2
Xm
X2
X1
T6
SWS
Y1
Y2
Yn
3
SCANNING LINE DRIVING CIRCUIT
5
CONTROL CIRCUIT
COLUMN DIRECTION
ROW DIRECTION

FIG.1

FIG.2

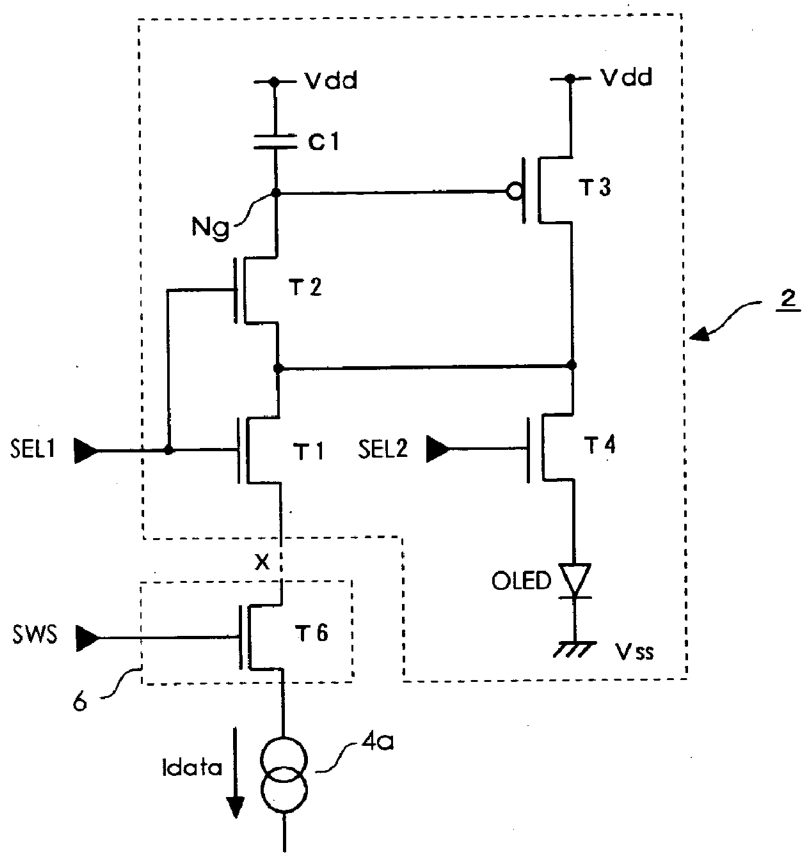
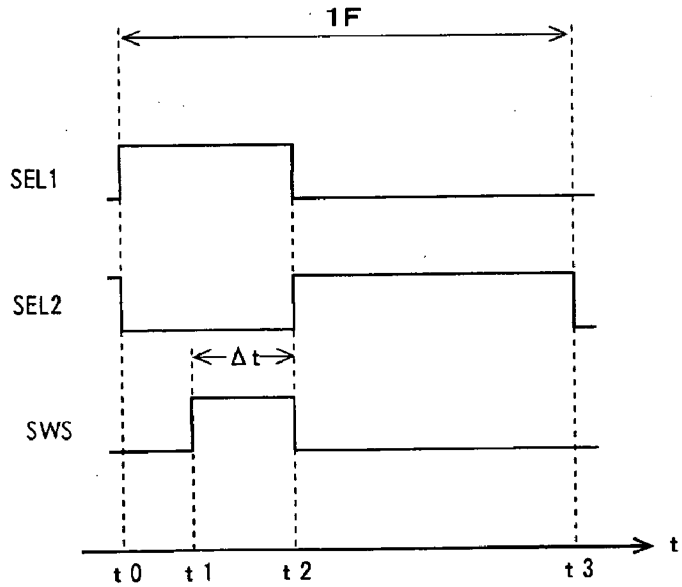

Vdd
Vdd
C1
T3
Ng
T2
2
SEL1
T1
SEL2
T4
X
OLED
SWS
T6
Vss
6
Idata
4a

FIG.3


1F
SEL1
SEL2
Δt
SWS
t
t0
t1
t2
t3

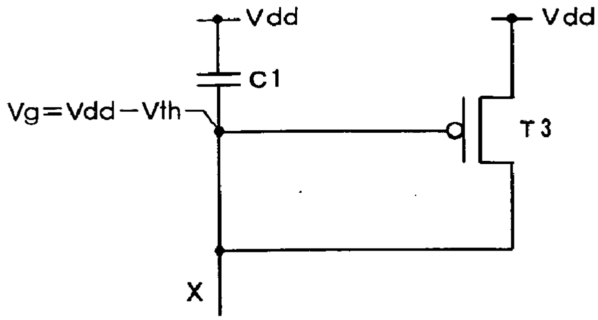


FIG.4A

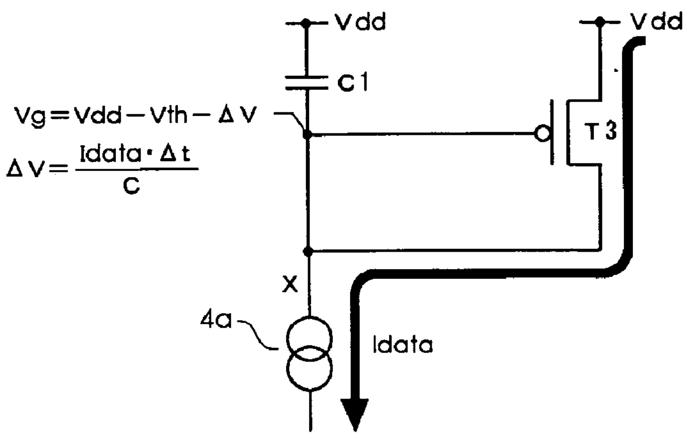


FIG.4B

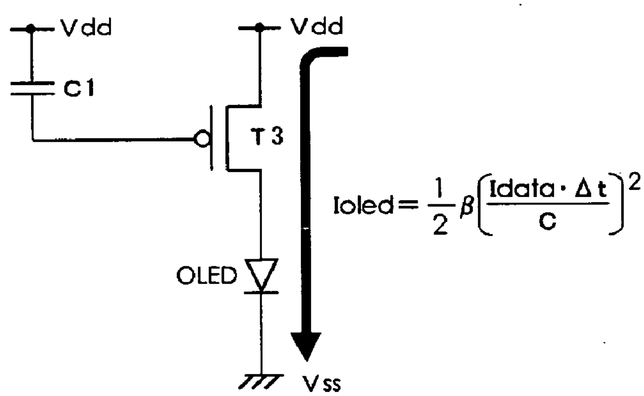
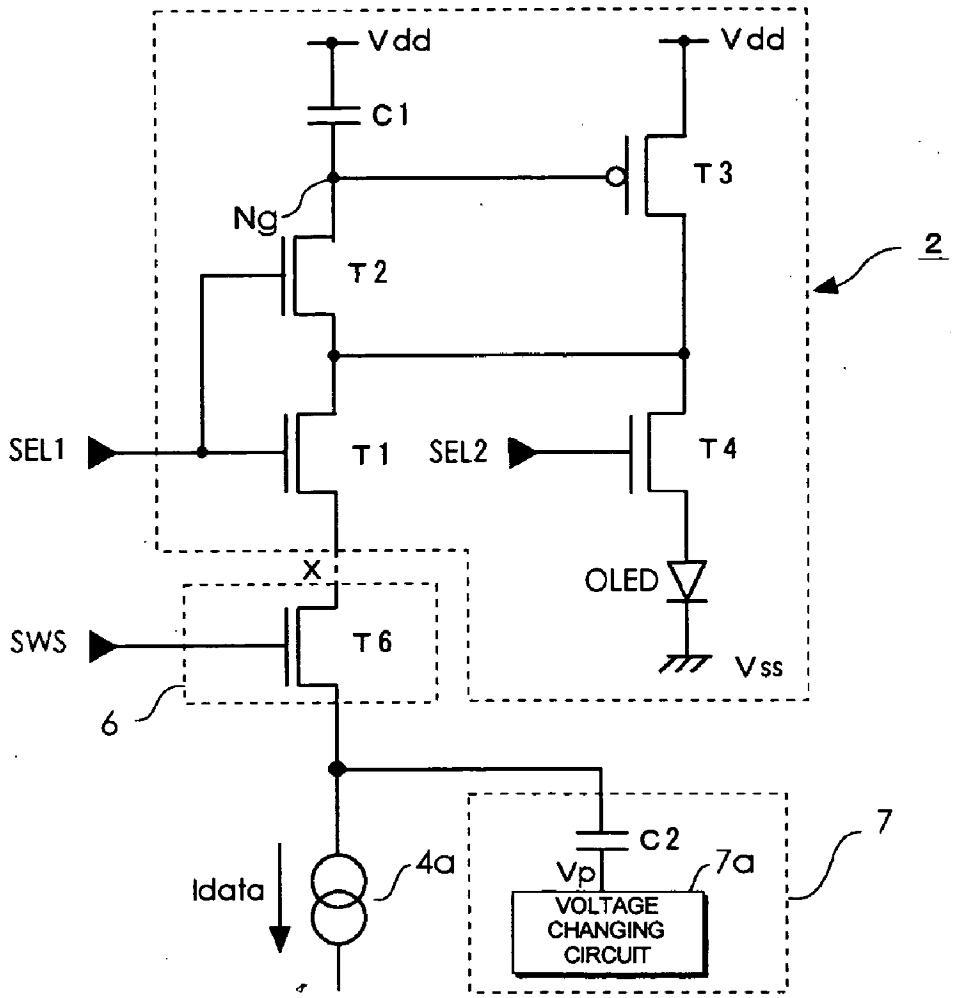


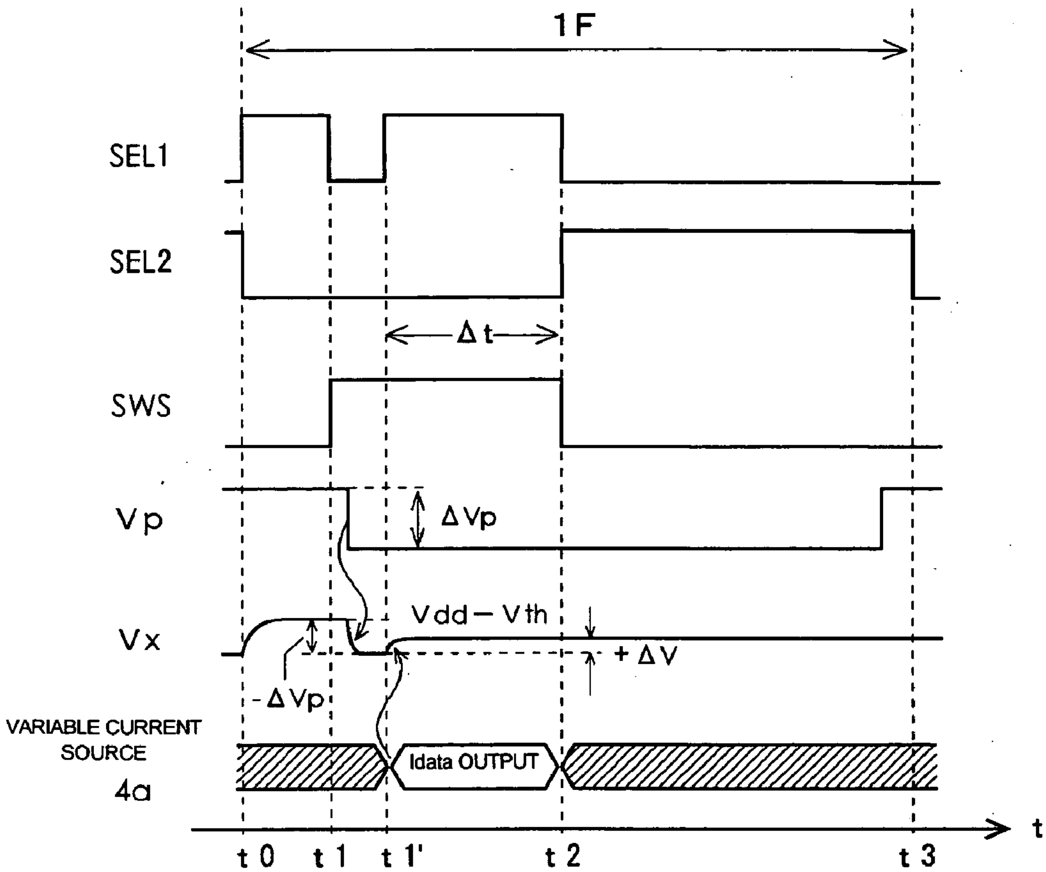
FIG.4C

FIG.5



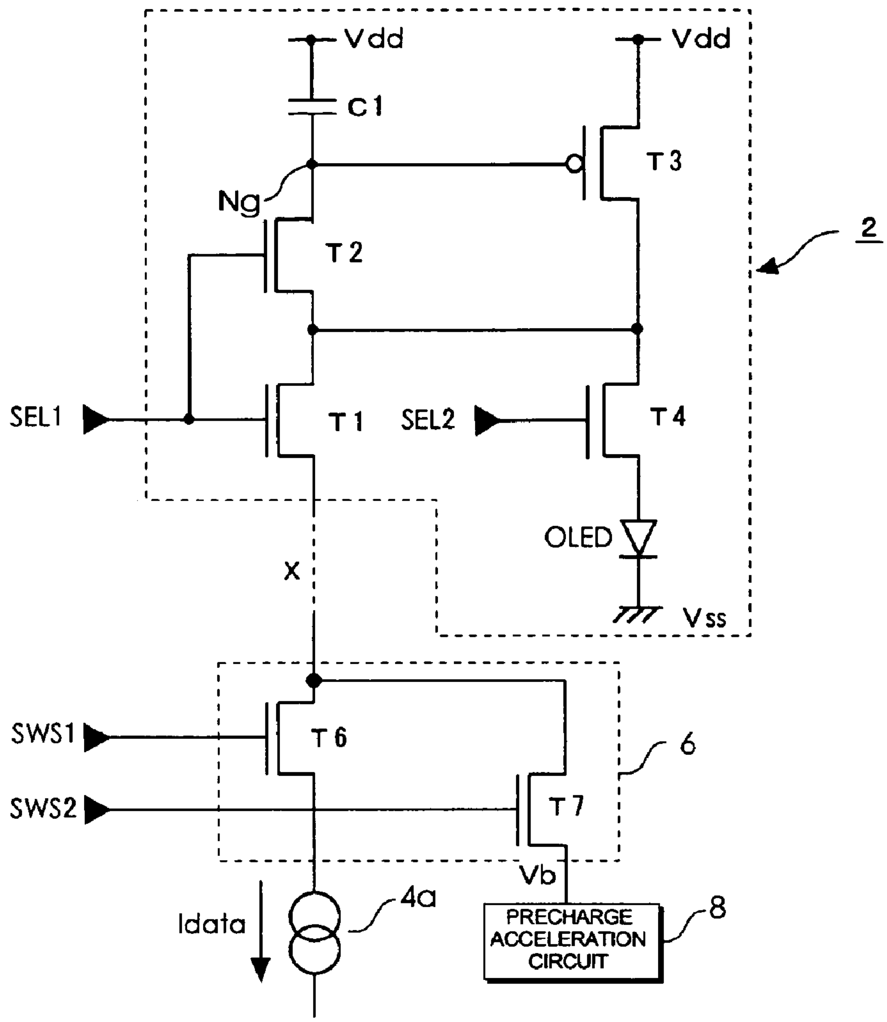
Vdd
Vdd
C1
T3
Ng
2
T2
SEL1
T1
SEL2
T4
X
OLED
SWS
T6
Vss
6
C2
7
4a
Vp
7a
Idata
VOLTAGE CHANGING CIRCUIT

FIG.6



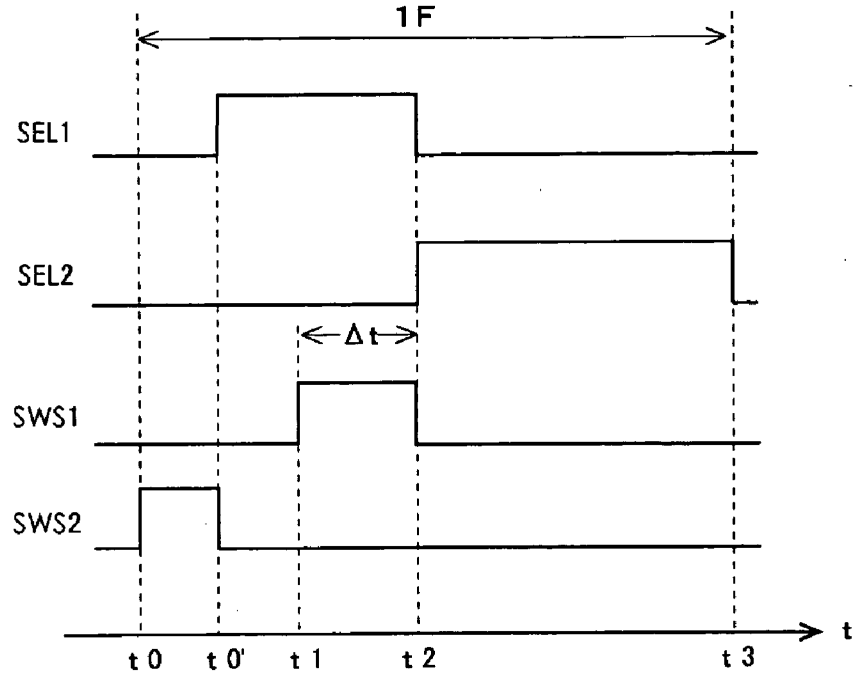
1F
SEL1
SEL2
Δt
SWS
Vp
ΔVp
Vx
Vdd − Vth
+ΔV
-ΔVp
VARIABLE CURRENT SOURCE
4a
Idata OUTPUT
t
t0
t1
t1'
t2
t3

FIG.7



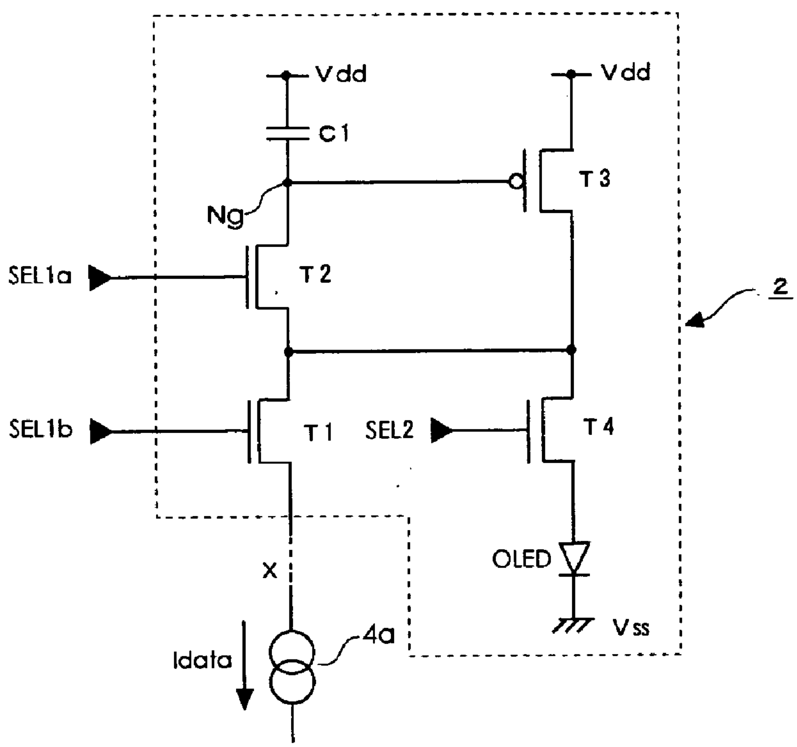
Vdd
Vdd
C1
T3
Ng
T2
2
SEL1
T1
SEL2
T4
OLED
X
Vss
SWS1
T6
6
SWS2
T7
Vb
4a
Idata
PRECHARGE ACCELERATION CIRCUIT
8

FIG.8



1F
SEL1
SEL2
Δt
SWS1
SWS2
t
t0
t0'
t1
t2
t3

FIG.9



Vdd
Vdd
C1
T3
Ng
SEL1a
T2
2
SEL1b
T1
SEL2
T4
OLED
X
Vss
4a
Idata

FIG.10

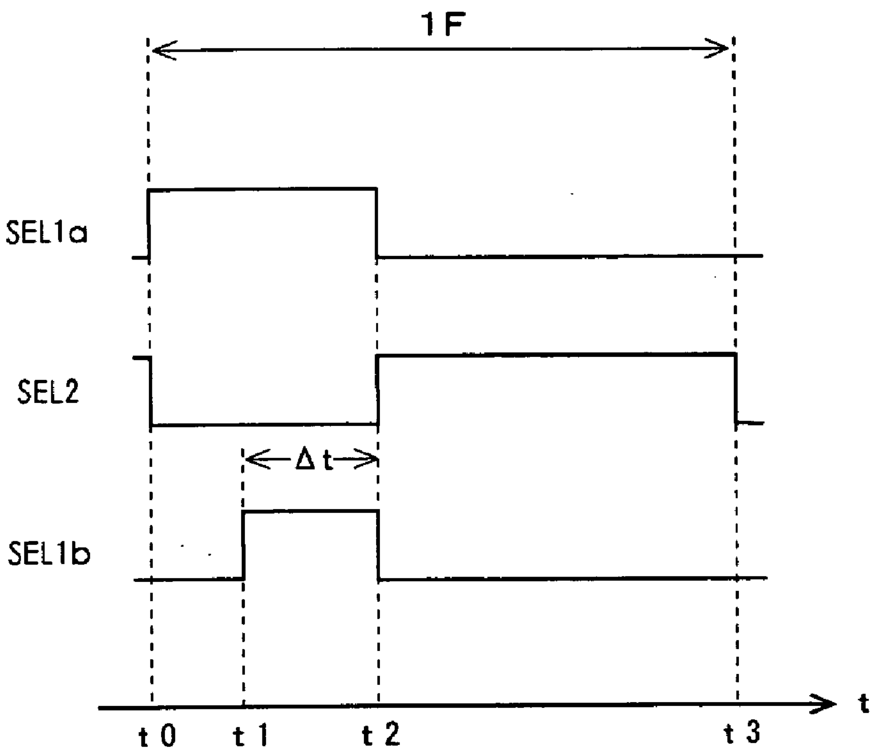


FIG.11

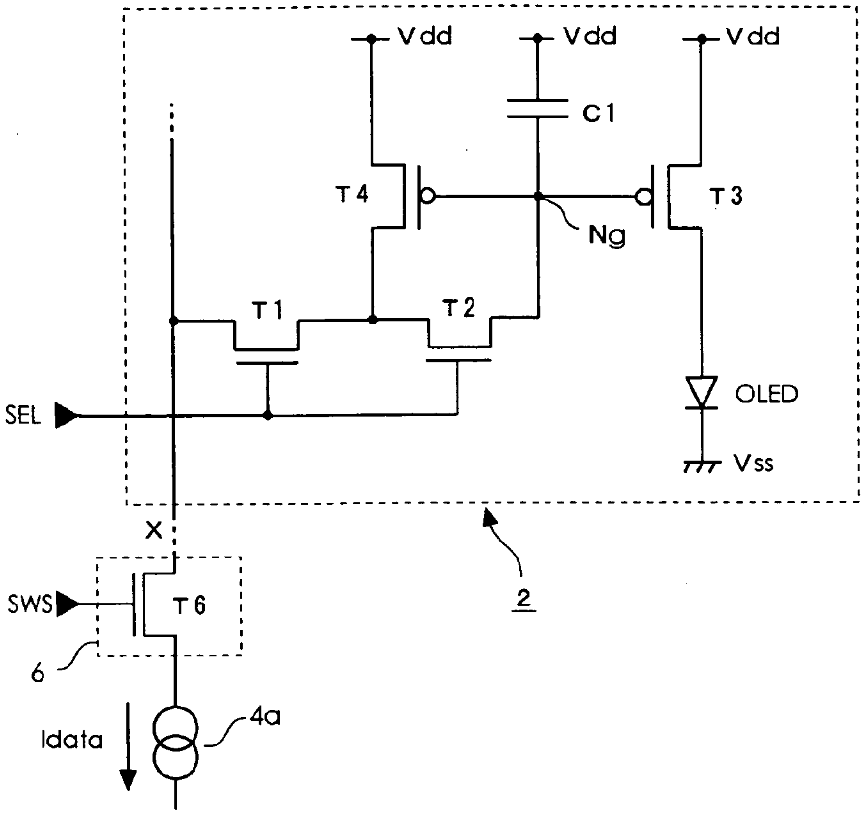
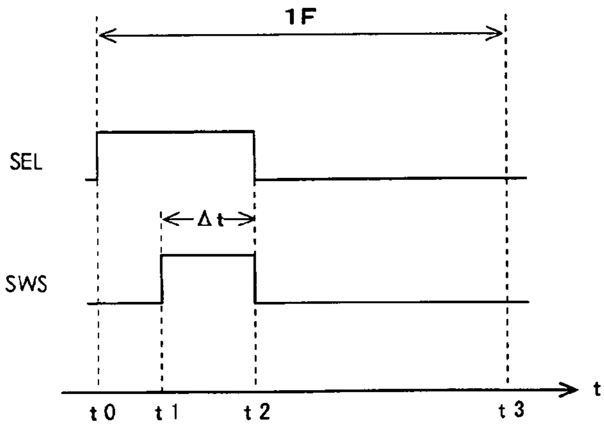

Vdd
Vdd
Vdd
C1
T4
T3
Ng
T1
T2
SEL
OLED
Vss
X
SWS
T6
2
6
Idata
4a

FIG.12


1F
SEL
Δt
SWS
t
t0
t1
t2
t3

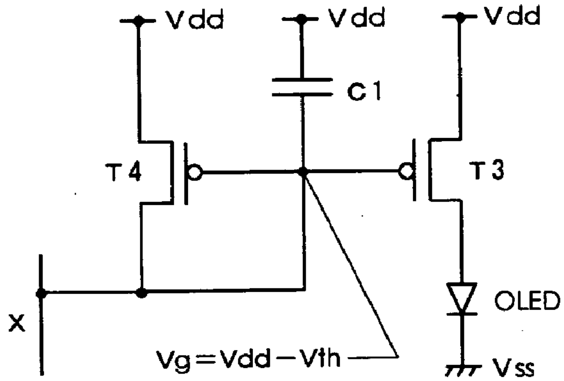


FIG.13A

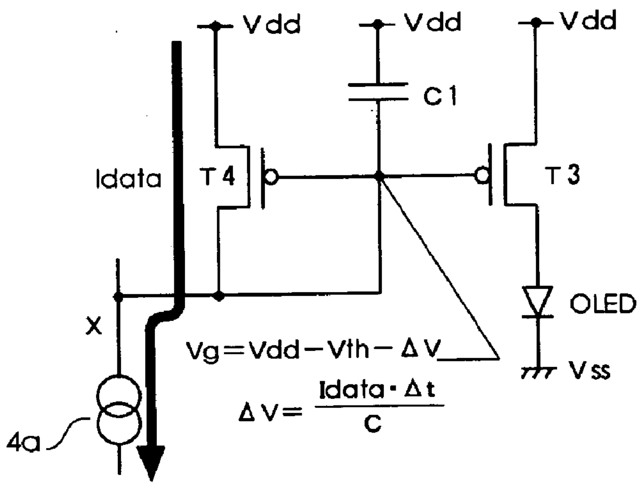


FIG.13B

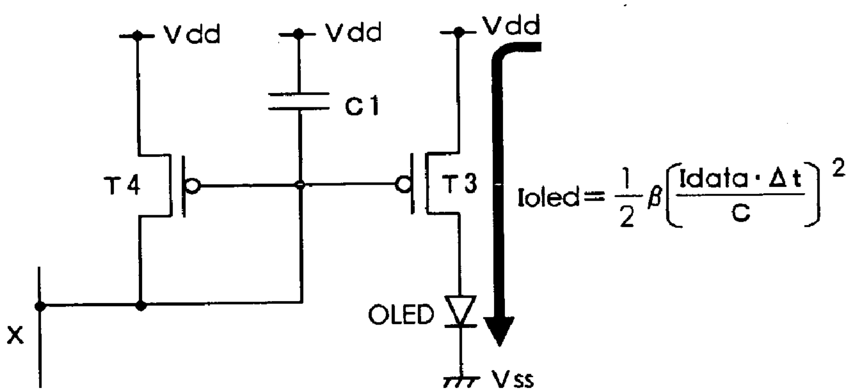


FIG.13C

FIG.14

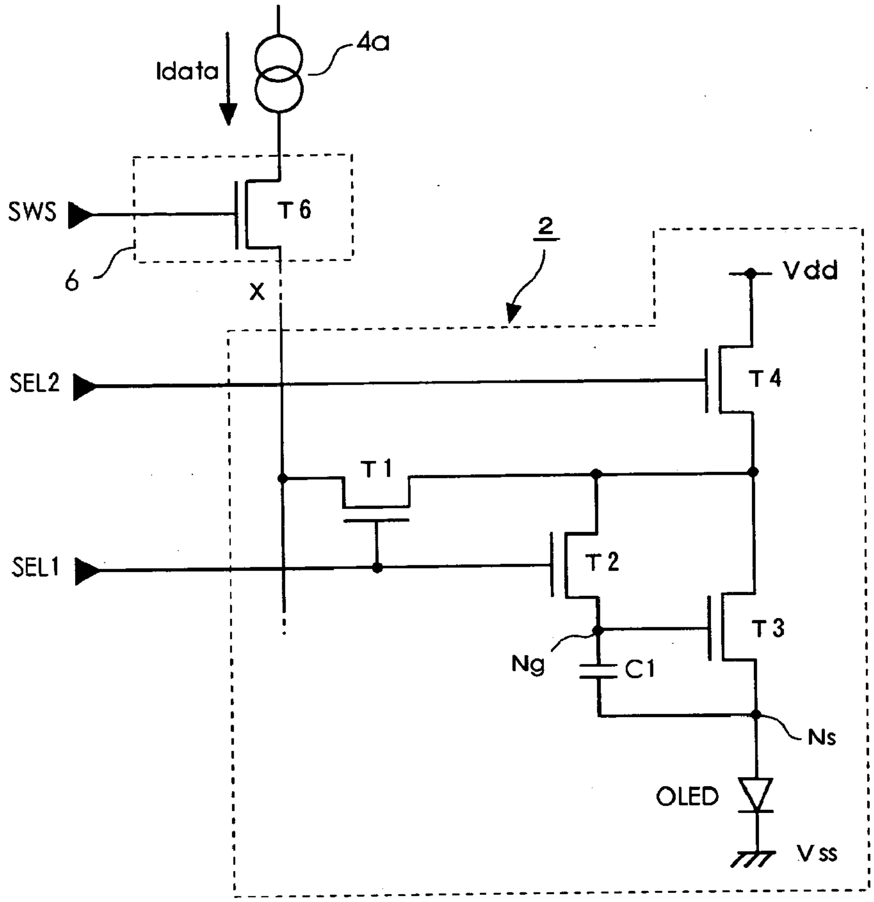
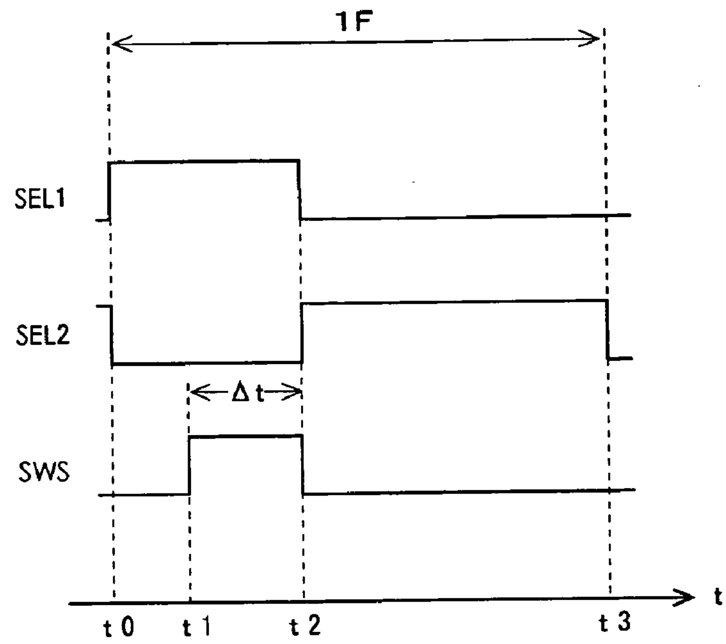


FIG.15



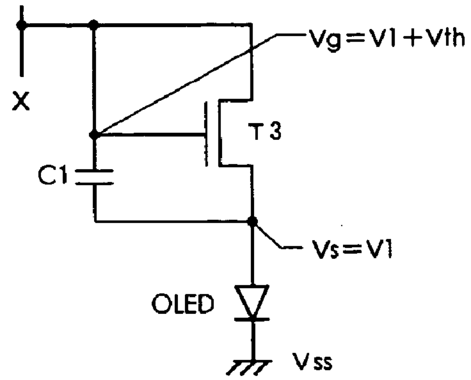


FIG.16A

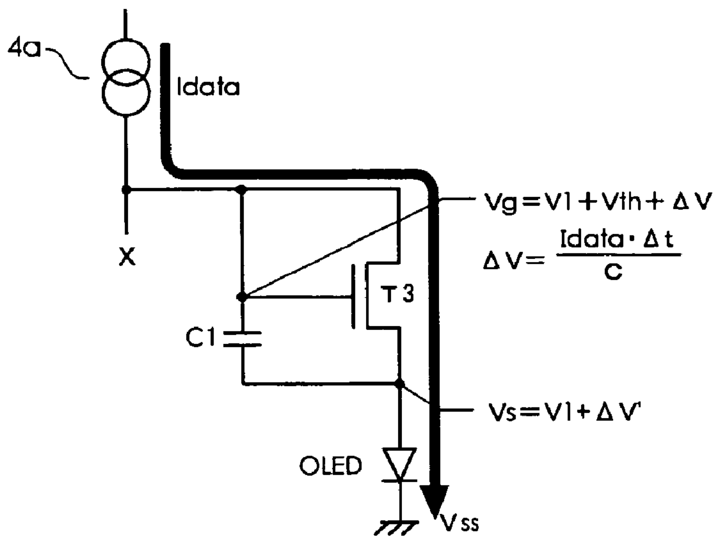


FIG.16B

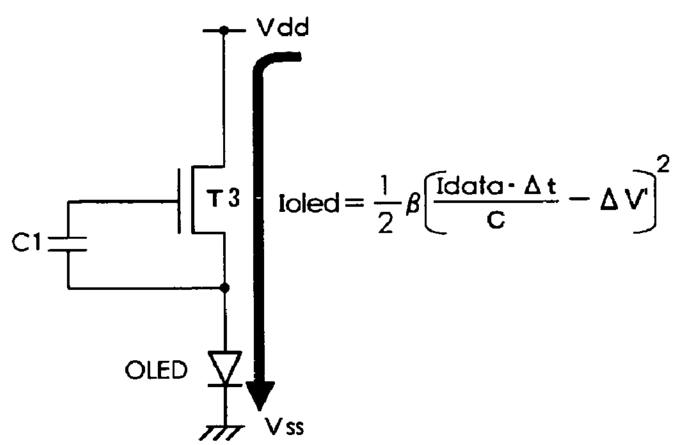
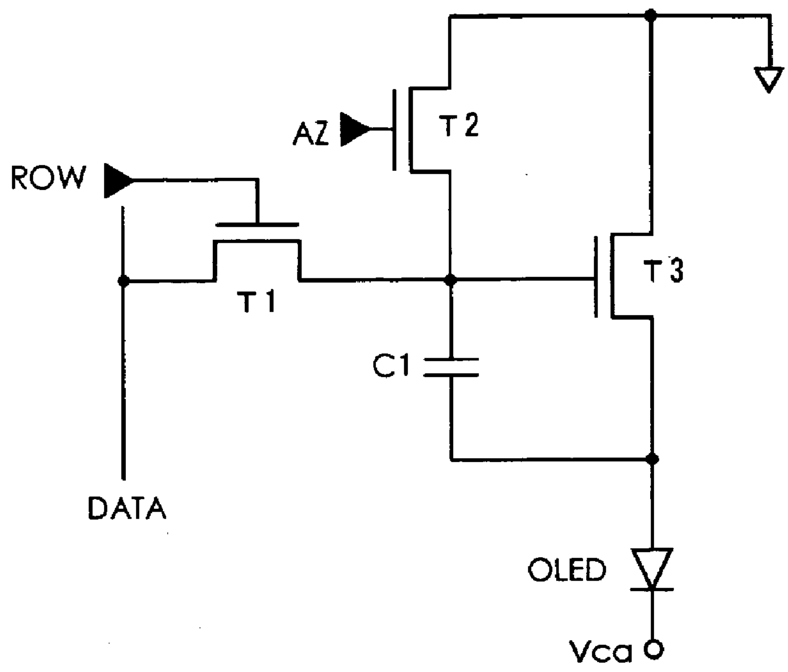


FIG.16C

FIG.17



PIXEL CIRCUIT, METHOD OF DRIVING THE SAME, AND ELECTRONIC APPARATUS

BACKGROUND OF THE INVENTION

[0001] 1. Field of Invention

[0002] The present invention relates to a pixel circuit, a method of driving the same, and electronic apparatus, and more specifically, it relates to a method of compensating Vth in a current-programmed method.

[0003] 2. Description of Related Art

[0004] Recently, displays using an organic electroluminescent (EL) element draw attention. The organic EL element is one of current-driven type elements in which the brightness is set according to a driving current flowing therethrough. A data supplying method to pixels using the organic EL element includes a voltage-programmed mode in which voltage-based data is supplied to data lines and a current-programmed mode in which current-based data is supplied to the data lines. In the voltage-programmed mode, a problem occurs that variation in a driving current depending on a threshold voltage (hereinafter, referred to as 'Vth') of a driving transistor may be caused, but conventionally, the solution is suggested.

[0005] **FIG. 17** is a diagram of a conventional voltage-programmed mode pixel circuit. The pixel circuit has an organic EL element OLED, a capacitor C**1** and three of n-channel type transistors T**1** through T**3**, in which the capacitor C**1** is provided between a gate and a source of the transistor T**3**. The pixel circuit operates as the following processes by means of a swing of a voltage Vca of an opposing electrode. First, if the transistor T**1** is turned off and the transistor T**2** is turned on, a cathode voltage Vca of the organic EL element OLED is set to −18V. Accordingly, since the transistor T**3** is turned on, an anode voltage of the organic EL element OLED becomes lower than −Vth (Vth is a threshold voltage of the transistor T**3**), and then a voltage higher than Vth is stored in the capacitor C**1**. Next, if the transistor T**2** is turned off, a gate of the transistor T**3** is in a floating state. Subsequently, if the cathode voltage Vca is set to 10V, a reverse bias voltage is applied to the organic EL element. Accordingly, the transistor T**3** is turned off, and then a gate voltage of the transistor T**3** becomes higher than Vth due to a change in the cathode voltage Vca. Subsequently, the transistor T**3** is turned on again, and then the anode of the organic EL element OLED becomes almost 0 V. In this state, if the transistor T**2** is turned on and the cathode voltage Vca is set to 0 V, the anode voltage of the organic EL element becomes sufficiently low due to a capacitive coupling to be settled to −Vth, and Vth is stored in the capacitor C**1**. Next, if the transistor T**1** is turned on and the transistor T**2** is turned off, a data voltage defining grayscale level of a pixel is supplied to the pixel circuit. If a self-capacitance of the organic EL element OLED is set to be sufficiently larger than that of the capacitor C**1**, the anode voltage of the organic EL element is maintained almost to −Vth when the cathode voltage Vca is 0 V, and in the capacitor C**1** a voltage of Vth+Vdata is stored. And then, the transistor T**1** and T**2** are turned off together, and the cathode voltage Vca is set to −18 V. At this time, since the voltage of Vth+Vdata is stored in the capacitor C**1**, a channel current (driving current) proportional to the voltage of Vth+Vdata flows through a channel of the transistor T**3**, whereby the organic EL element OLED is emitted. In such manner, if Vth is previously stored in the capacitor C**1** and data is written based on Vth, variation in Vth of the transistor T**3** can be compensated, and further a driving current independent of Vth can be generated.

SUMMARY OF THE INVENTION

[0006] Meanwhile, the current-programmed mode, unlike the voltage-programmed mode, is generally advantageous in that an uniform driving current independent of Vth of a driving transistor can be generated. For this reason, the current-programmed mode is widely adopted. However, the current-programmed mode is made on the assumption that current-based data (current data) is written completely within a predetermined data writing period. Accordingly, if the data writing is not completed within the predetermined period, that is, the data writing is lacking, when the same grayscale is displayed, the driving current which must be primarily the same for every driving transistor may be differentiated depending on variation in Vth. This may be generated in a large-sized display in which a parasitic capacitance of a data line is very large and a high-definition display in which the number of scanning lines is numerous and a data writing period is not sufficiently secured. Further, in the case that a current to be programmed in a pixel is very small (when using high efficient EL element or phosphorescence material, the above problem may also occur. Besides, in the case that a security of a contrast ratio is preceded, for design convenience, lack writing in a low-resolution grayscale region may be tolerated at a certain degree, and the current to be programmed may be set in a wider range.

[0007] The present invention has been made in consideration of the above problems, and its object is to suppress variation in a driving current depending on Vth in a current-programmed mode pixel circuit.

[0008] In order to solve the above problems, there is provided a method of driving a pixel circuit according to a first aspect of the present invention. The driving method comprises: a first step of setting a gate voltage of a diode-connected first transistor to an offset voltage according to a threshold voltage of the first transistor, in a state in which a variable current source variably generating a data current is electrically isolated from the first transistor, a second step of writing, in a capacitor connected to a gate of the diode-connected first transistor, data set based on the offset voltage and according to a product of the data current supplied from the variable current source via data lines and a supply time thereof, in a state in which the variable current source and the first transistor are electrically connected to each other, and a third step of generating a driving current according to the data stored in the capacitor by a second transistor whose gate is connected to the capacitor to set brightness of an electro-optical device.

[0009] In the first aspect, a transistor rolls as both the first transistor and the second transistor. Further, the first transistor and the second transistor may constitute a current mirror.

[0010] Further, in the first aspect, preferably, the first step comprises a step of turning off a switching element provided between the variable current source and the first transistor, and the second step comprises a step of turning on the switching element. Further, in the first aspect, the driving

method may further comprise a fourth step of regulating the offset voltage set in the first step, by variably controlling the terminal voltage of a capacitor that another terminal is coupled to the data lines.

[0011] In this case, the amount of change of the terminal voltage of a capacitor in the fourth step is set according to a grayscale level to be displayed.

[0012] Further, the driving method may comprise, prior to setting the offset voltage in the first step, a fifth step of supplying, to the data lines, a predetermined voltage having a voltage level that turns on the first transistor.

[0013] More, there is provided a pixel circuit according to a second aspect of the present invention. The pixel circuit comprises: a first transistor normally or selectively diode-connected through a control of a switching transistor, for generating data according to data current supplied from a variable current source via the data lines, a capacitor connected to a gate of the first transistor, in which data generated by the first transistor is written, a second transistor, whose gate is connected to the capacitor, for generating a driving current according to data stored in the capacitor, and an electro-optical element in which the brightness is set according to the driving current generated by the second transistor. Here, the first transistor sets its gate voltage to an offset voltage according to its threshold voltage in a state which the first transistor is electrically isolated from the variable current source. Further, in a state which the first transistor is electrically connected to the variable current source, the first transistor writes data set based on the offset voltage and according to a product of the data current supplied from the variable current source and a supply time thereof, in the capacitor.

[0014] In the second aspect, a transistor may rolls as both the first transistor and the second transistor. Further, the first transistor and the second transistor may constitute a current mirror.

[0015] Further, in the second aspect, the pixel circuit may further comprises a switching circuit for electrically isolating between the variable current source and the data line for a period during which the gate voltage is set to the offset voltage, and electrically connecting between the variable current source and the data line for a period during which the data is written in the capacitor. Further, the pixel circuit may further comprise a precharge regulation circuit that regulate the offset voltage by variably controlling the terminal voltage of a capacitor that another terminal is coupled to the data lines. In this case, the precharge regulation circuit preferably controls the amount of change of the terminal voltage of a capacitor according to a grayscale level to be displayed. In addition, the pixel circuit may further comprise a precharge acceleration circuit for supplying, to the data lines, a predetermined voltage having a voltage level that turns on the first transistor, prior to a period during which the gate voltage is set to the offset voltage.

[0016] More, there is provided an electronic apparatus according to a third aspect of the present invention. The electronic apparatus comprises an electro-optical device having a pixel circuit according to the second aspect of the present invention.

[0017] In the present invention, the gate voltage of the first transistor is previously set to the offset voltage, and the data writing to the capacitor is made in the current-programmed mode. Data to be written is set based on the offset voltage previously set and according to the product of the data current and the supply time thereof. Thus, when the driving current is generated based on data stored in the capacitor, it is possible to reduce a dependency on Vth of the driving current. As a result, even when data writing is lacking, it is possible to generate an uniform driving current, and thus it is possible to set the electro-optical device to have a desirable brightness.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] **FIG. 1** is a block diagram showing a configuration of an electro-optical device;

[0019] **FIG. 2** is a diagram of a pixel circuit according to a first embodiment;

[0020] **FIG. 3** is a timing chart of operation according to the first embodiment;

[0021] **FIG. 4** is an explanatory view of the operation according to the first embodiment;

[0022] **FIG. 5** is a diagram of a pixel circuit according to a second embodiment;

[0023] **FIG. 6** is a timing chart of operation according to the second embodiment;

[0024] **FIG. 7** is a diagram of a pixel circuit according to a third embodiment;

[0025] **FIG. 8** is a timing chart of operation according to the third embodiment;

[0026] **FIG. 9** is a diagram of a pixel circuit according to a fourth embodiment;

[0027] **FIG. 10** is a timing chart of operation according to the fourth embodiment;

[0028] **FIG. 11** is a diagram of a pixel circuit according to a fifth embodiment;

[0029] **FIG. 12** is a timing chart of operation according to the fifth embodiment;

[0030] **FIG. 13** is an explanatory view of the operation according to the fifth embodiment;

[0031] **FIG. 14** is a diagram of a pixel circuit according to a sixth embodiment;

[0032] **FIG. 15** is a timing chart of operation according to the sixth embodiment;

[0033] **FIG. 16** is an explanatory view of the operation according to the sixth embodiment;

[0034] **FIG. 17** is a diagram of a conventional pixel circuit.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

First Embodiment

[0035] **FIG. 1** is a block diagram showing a configuration of an electro-optical device according to the present embodiment. A display unit **1** is, for example, an active matrix type display panel in which the electro-optical device is driven by

a TFT (thin film transistor). In the display unit **1**, m dots by n lines of a group of pixels are arranged in a matrix (in a two-dimensional plan view). In the display unit **1**, a group of scanning lines **Y1** through Yn each extending in a horizontal direction and a group of data lines **X1** through Xm each extending in a vertical direction are provided, and pixels **2** are arranged in correspondence with intersections of the scanning lines and the data lines. Moreover, while in a monochromatic panel, one pixel corresponds to one pixel circuit described below, when one pixel comprises three R, G, B sub-pixels like a color panel, one sub-pixel corresponds to one pixel circuit. Further, as regards the configuration of the pixel circuit described below, one scanning line may represent a respective one of scanning lines (**FIG. 11**) or may represent a set of plural scanning lines (**FIGS. 2, 5, 7, 9** and **14**).

[**0036**] A control circuit **5** synchronously controls a scanning line driving circuit **3**, a data line driving circuit **4** and a switching circuit **6** based on a vertical synchronizing signal Vs, a horizontal synchronizing signal Hs, a dot clock signal DCLK, grayscale data D, and so on, which are inputted from preceding devices. Under the synchronous control, the scanning line driving circuit **3**, the data line driving circuit **4** and the switching circuit **6** cooperate with each other to control a display on the display unit **1**.

[**0037**] The scanning line driving circuit **3** mainly comprises shift registers, output circuits, and so on, and outputs a scanning signal SEL to the scanning lines **Y1** through Yn to perform a line sequential scanning. The scanning signal SEL is a two-level signal of a high potential level (hereinafter, referred to as 'H level') and a low potential level (hereinafter, referred to as 'L level'). A scanning line corresponding to a row of pixels to which data is written is set to H level and other scanning lines are set to L level. The scanning line driving circuit **3** performs the line sequential scanning for selecting each scanning line Y in a predetermined order (in general, from top to bottom) for every period (**1**F) in which images of one frame are displayed. Meanwhile, the data line driving circuit **4** has mainly shift registers, line latch circuits, output circuits, and so on. In the present embodiment, if the current-programmed mode is adopted, the data line driving circuit **4** comprises a variable current source (**4***a* in **FIG. 2**) for variably generating a data current Idata based on grayscale data defining grayscale level to be displayed in the pixel **2**. In one horizontal scanning period (**1**H) corresponding to the period in which one scanning line is selected, the data line driving circuit **4** simultaneously outputs the data current Idata to a row of pixels to which current data is written, and at the same time, latches in a point sequential manner data relevant to a row of pixels to be written in next one horizontal scanning period (**1**H). In any horizontal scanning period (**1**H), m data corresponding to the number of data lines X are sequentially latched. And then, in next one horizontal scanning period (**1**H), the latched m data are converted into current data Idata by means of the variable current source, and are simultaneously output to the corresponding data lines. Further, the switching circuit **6** comprising m switching elements, more specifically, m switching transistors **T6** corresponding to the data lines **X1** through Xm. The transistors **T6** provided by one for every data line are, for example, n-channel type transistors and are commonly controlled by a single switching signal SWS outputted from the control circuit **5**. This control is performed in synchronization with the line sequential scanning by means of the scanning line driving circuit **3**.

[**0038**] **FIG. 2** is a diagram of a current-programmed mode pixel circuit according to the present embodiment. One pixel **2** comprises an organic EL element OLED, four transistors **T1** through **T4** as an active element, and a capacitor **C1** storing data. The organic EL element represented as a diode is a typical current-driven type element in which the brightness is set by a current Ioled flowing therethrough. In this configuration example, the n-channel type transistors **T1, T2** and **T4** and the p-channel type transistor **T3** are used, but it is just an example. Thus, the channel types of the respective transistors **T1** through **T4** may be set differently from the above channel type combination. Further, between the data line X connected to the pixel **2** and the variable current source **4***a* constituting a portion of the data line driving circuit **4**, a single switching transistor **T6** provided by one for every data line is connected. In the present specification, as regards a three-terminal type transistor having a source, a drain and a gate, one of the source and drain is referred to as 'one terminal' and the other is referred as 'the other terminal'.

[**0039**] A gate of the switching transistor **T1** is connected to one scanning line to which a first scanning signal SEL**1** is supplied, and one terminal of the switching transistor **T1** is connected to one data line X to which the data current Idata is supplied. The other terminal of the switching transistor **T1** is commonly connected to one terminal of the switching transistor **T2**, one terminal of the driving transistor **T3** and one terminal of the driving transistor **T4**. A gate of the switching transistor **T2** is connected to the scanning line to which the first scanning signal SEL**1** is supplied, like the first switching transistor **T1**. The other terminal of the switching transistor **T2** is connected to a node Ng to which one electrode of the capacitor **C1** and a gate of the driving transistor **T3** are commonly connected. To the other electrode of the capacitor **C1** and the other terminal of the driving transistor **T3**, a Vdd terminal is connected, through which a power source voltage is constantly supplied. The switching transistor **4** is provided between one terminal of the driving transistor **T3** of which a gate is supplied with a second scanning signal SEL**2** and an anode of the organic EL element OLED. A cathode of the organic EL element OLED is connected to a Vss terminal to which a reference voltage Vss lower than the power source voltage Vdd is constantly supplied. Moreover, in this configuration example, the driving transistor **T3** functions a programming element for wiring data according to the data current Idata in the capacitor **C1**, as well as a driving element for generating the driving current Ioled primarily.

[**0040**] **FIG. 3** is a timing chart of operation of the pixel circuit shown in **FIG. 2**. In a period t**0** to t**3** corresponding to one frame period (**1**F) described above, consecutive processes are generally divided into a precharge process in an initial period t**0** to t**1**, a data writing process in a subsequent period t**1** to t**2**, and a driving process in a last period t**2** to t**3**.

[**0041**] First, in the precharge period t**0** to t**1**, a precharge to be completed within the pixel **2** is performed, and by means of this precharge, a Vth compensation of the driving transistor **T3** is performed. More specifically, the level of the

first scanning signal SEL1 becomes H level, and then the switching transistors T1 and T2 are turned on together. Accordingly, the data line and one terminal (drain) of the driving transistor T3 are electrically connected to each other, and thus the driving transistor T3 becomes a diode-connection in which its gate and its drain are electrically connected to each other. In this period t0 to t1, since the level of the switching signal is L level and the switching transistor T6 is turned off, the node Ng in the pixel 2 and the variable current source 4*a* are still electrically isolated from each other. Further, the level of the second scanning signal SEL2 becomes L level, and then the switching transistor T4 is turned off. Accordingly, as shown in **FIG. 4**(*a*), in a state in which the node Ng and the variable current source 4*a* are electrically isolated from each other, the precharge of the capacitor C1 and the data line X is performed by means of the power source voltage Vdd of the Vdd terminal. By means of this precharge, a voltage of the node Ng, that is, a gate voltage Vg of the driving transistor T3 is set to an offset voltage (Vdd−Vth), and its voltage level is principally determined by means of the threshold voltage Vth of the driving transistor T3. In such manner, prior to writing data, the voltage Vg of the node Ng is forcibly offset from a voltage level depending on data written in the driving process of the previous one frame period (1F), to the offset voltage (Vdd−Vth) corresponding to a precharge level. Moreover, in this period t0 to t1, since the switching transistor T4 is turned off, the organic EL element OLED does not emit.

[0042] Next, in the data writing period t1 to t2, based on the offset voltage (Vdd−Vth) set in the previous precharge period t0 to t1, the data is written in the capacitor C1. In this period t1 to t2, since the scanning signals SEL1 and SEL2 are respectively at the same level as those in the precharge period t0 to t1, the switching transistors T1 and T2 are left to be turned on, and the switching transistor T4 is left to be turned off. Further, in the timing t1, the level of the switching signal SWS rises to H level, and then the switching transistor T6 which is turned off is switched to be turned on. In such manner, as shown in **FIG. 4**(*b*), the node Ng and the variable current source 4*a* are electrically connected to each other. As a result, a path of the data current Idata is formed, and the path is made in a sequence of the Vdd terminal, a channel of the driving transistor T3 and the variable current source 4*a* (correctly speaking, channels of the switching transistors T1 and T6 also are included). The voltage Vg of the node Vg is calculated by means of the following equation 1.

$$Vg=Vdd-Vth-\Delta V$$
$$\Delta V=(Idata\cdot\Delta t)/C \quad \text{(Equation 1)}$$

[0043] Here, Idata is a voltage level of the data current Idata generated by the variable current source 4*a*, Δt is a time in the data writing period t1 to t2, that is, a supply time of the data current Idata. Further, a coefficient C is a total capacitance relating to a driving path of the data current Idata including a wiring capacitance of the data line X and a capacitance of the capacitor C1. As seen from the equation 1, the voltage Vg is changed by ΔV based on the offset voltage (Vdd−Vth), and the ΔV is principally specified according to a product of the data current Idata and its supply time Δt. Thus, in the capacitor C1, charges according to the voltage Vg are written as data. Moreover, in the period t1 to t2, like the previous precharge period t0 to t1, the switching transistor T4 is left to be turned off, and thus the organic EL element OLED does not emit.

[0044] Further, in the driving period t2 to t3, the driving current Ioled corresponding to a channel current of the driving transistor T3 is supplied to the organic EL element OLED, whereby the organic EL element is emitted. More specifically, levels of the first scanning signal SEL1 and the switching signal SWS fall to L level, the switching transistors T1, T2 and T6 are turned off together. Accordingly, the node Ng is electrically isolated from the variable current source 4*a*. However, even after the electrical isolation, to the gate of the driving transistor T3, a voltage according to data stored in the capacitor C1 is continuously applied. Further, in 'synchronization' with the falling of the first scanning signal SEL1, the level of the second scanning signal SEL2 rises to H level. In the present specification, the term 'synchronization' is used to represent a tolerable time offset to a margin for design as well as the same timing. In such manner, as shown in **FIG. 4**(*c*), along a sequential path of the Vdd terminal, the channel of the driving transistor T3, the organic EL element OLED and the Vss terminal, the driving current Ioled flows. On an assumption that the driving transistor T3 operates in a saturation region, the driving current Ioled (a channel current Isd of the driving transistor T3) flowing through the organic EL element OLED is calculated by the following equation 2. In the equation 2, a Vsg is a voltage between the gate and the source of the driving transistor T3. Further, a gain coefficient β is principally specified by a mobility μ of carrier, a gate capacitance A, a channel width W and a channel length L of the driving transistor T3 ($\beta=\mu A\,W/L$).

$$Ioled=Isd=\tfrac{1}{2}\beta(Vsg-Vth)^2 \quad \text{(Equation 2)}$$

[0045] Here, if the Vg calculated by the equation 1 is substituted for the gate voltage of the driving transistor T3, the equation 2 is transformed to the following equation 3.

$$Ioled=\tfrac{1}{2}\beta(Vs-Vg-Vth)^2=\tfrac{1}{2}\beta\{Vdd-(Vdd-Vth-\Delta V)-Vth\}^2=\tfrac{1}{2}\beta\cdot\Delta V^2=\beta/2(Idata\cdot\Delta t/C)^2 \quad \text{(Equation 3)}$$

[0046] In the equation 3, it is important that the Vths are balanced each other during the equation transformation. This means that the driving current Ioled to be generated by the driving transistor T3 does not depend on the Vth. The emitting brightness of the organic EL element OLED is principally determined by the driving current Ioled according to the product of the data current Idata and its supply time Δt, and thus grayscale level of the pixel 2 is set.

[0047] In such manner, in the present embodiment, in the precharge prior to the data writing, the voltage of the node Ng is set to the offset voltage (Vdd−Vth) and data is written in the capacitor C1 based on the product of the data current Idata and its supply time Δt. In general, variation in the Vth is larger than that of the Δt or the C, and therefore, by compensating the Vth, the degree of the precharge in each pixel 2 becomes equivalent even when characteristics of the driving transistor T3 in the display unit 1 are uneven. As a result, even in the case that the data writing is lacking as describe above, it is possible to suppress variation in the driving current depending on the Vth and thus improve display quality still more.

[0048] Further, according to the present embodiment, it is possible to perform the precharge to be completed within the pixel 2, without providing an additional circuit for precharge outside the pixel 2. This is advantageous for simplifying a configuration of the circuit or reducing the power consumption.

Second Embodiment

[0049] The present embodiment relates to a technique for regulating the offset voltage (Vdd−Vth) corresponding to the precharge level according to a grayscale level to be displayed, based on the basic configuration of the first embodiment described above. **FIG. 5** is a diagram of a pixel circuit according to the present embodiment. The pixel circuit has a feature that a precharge regulation circuit **7** is added to the pixel circuit shown in **FIG. 2**, and other elements are the same as those of the pixel circuit of **FIG. 2**. Thus, the descriptions of like elements will be omitted. The precharge regulation circuit **7** comprises a capacitor C**2** and a voltage changing circuit **7***a* for variably setting an output voltage Vp. To one electrode of the capacitor C**2**, one terminal of the switching transistor T**6** constituting a portion of the switching circuit **6** and a connecting terminal with the variable current source **4***a* are connected. Further, to the other electrode of the capacitor **2**, an output terminal of the voltage changing circuit **7***a* is connected, and then a voltage level of the voltage Vp of the output terminal is variably controlled according to grayscale.

[0050] **FIG. 6** is a timing chart of operation of the pixel circuit shown in **FIG. 5**. A period t**0** to t**3** corresponding to one frame period (**1**F) is generally divided into a precharge period t**0** to t1, a precharge regulation period t1 to t**1**', a data writing period t**1**' to t**2** and a driving period t**2** to t**3**. The present embodiment is different from the first embodiment in that the precharge regulation period t1 to t**1**' is provided between the precharge period t**0** to t1 and the data writing period t**1**' to t**2**, but other processes are basically the same as those of the first embodiment. The variable current source **4***a*, in the data writing period t**1**' to t**2**, outputs the data current Idata to the data line X, and, in other periods, is set to a state of high impedance, that is, a state which is electrically isolated from the pixel **2**.

[0051] First, in the precharge period t**0** to t**1**, the level of the first scanning signal SEL1 becomes H level, and thus the driving transistor T**3** is diode-connected and the data line X and the node Ng are electrically connected to each other. Further, in this period t**0** to t**1**, since the level of the switching signal SWS is L level, and the switching transistor T**6** is turned off, the data line X is electrically isolated from the variable current source **4***a* and the precharge regulation circuit **7**. Accordingly, the capacitor C**1** and the data line X are precharged, the voltage Vg of the node Ng and a voltage Vx of the data line X are set to the offset voltage (Vdd−Vth) as the precharge level.

[0052] In the next precharge regulation period t**1** to t**1**', the level of the first scanning signal SEL**1** becomes temporally L level, and thus the switching transistors T**1** and T**2** are turned off together. At the same time, the level of the switching signal SWS becomes H level, and thus the switching transistor T**6** is turned on. In this period t**1** to t**1**', while maintaining the variable current source **4***a* as high impedance state, the previously set precharge level (Vdd−Vth) is regulated. More specifically, in any timing of this period t**1** to t**1**', the voltage changing circuit **7***a* which is a portion of the precharge regulation circuit **7** lowers the output voltage Vp by ΔVp stepwise from a current voltage level. Accordingly, on an assumption that a wiring capacitance of the data line X is sufficiently larger than a capacitance of the capacitor C**2**, the voltage Vx of the data line X which is capacitively coupled via the capacitor C**2** is lowered by ΔVp (Vx=Vdd−Vth−ΔVp) based on the previously set offset voltage (Vdd−Vth). Here, ΔVp which corresponds to a regulation amount of the precharge level is variably set according to a grayscale level of the pixel **2** to be displayed next time. That is, in low-resolution grayscale in which the data current Idata is relatively small, ΔVp becomes small, and then the voltage Vx (precharge level) of the data line X is set to be high. In such manner, in the subsequent data writing process, a load required for charging the data line X and the capacitor C**1** can be reduced, and further a lack data writing can be suppressed. Meanwhile, in high-resolution grayscale in which the data current Idata is relatively large, ΔVp becomes larger than that of the low-resolution grayscale, and then the precharge level is set to be low.

[0053] In the subsequent data writing period t**1**' to t**2**, the level of the first scanning signal SEL1 rises to H level again, and thus the node Ng and the variable current source **4***a* are electrically connected to each other. Accordingly, the data writing based on the offset voltage (Vdd−Vth) is performed. In such manner, the voltage Vx of the data line X rises or falls by a voltage value ΔV depending on the data current Idata, based on the previously set voltage (Vdd−Vth−ΔVp). Further, in the driving period t**2** to t**3**, the driving current Ioled generated by the driving transistor T**3** flows in the organic EL element OLED, whereby the organic EL element OLED is emitted. Similarly to the first embodiment, the driving current Ioled is specified by the product of the data current Idata and its supply time Δt, and does not depend on the Vth of the driving transistor T**3**.

[0054] As described above, according to the present embodiment, similarly to the first embodiment, it is possible to suppress variation in the driving current Ioled depending on the Vth of the driving transistor T**3**. Further, in the present embodiment, the precharge level is regulated according to a grayscale level of the pixel **2** to be displayed. Accordingly, it is possible to perform efficiently the data writing over all of grayscale regions without causing the lack data writing. Moreover, in the present embodiment, the regulation of the precharge level may be set regardless of grayscale level of the pixel **2** to be displayed, that is, may function so as to change simply a value of the offset voltage. In this case, the precharge regulation circuit **7** can be simplified.

[0055] Moreover, the precharge regulation technique described in the present embodiment can be applied similarly to pixel circuits according to fifth and sixth embodiments described below.

Third Embodiment

[0056] The present embodiment relates to a technique for accelerating the precharge, based on the basic configuration of the first embodiment described above. **FIG. 7** is a diagram of a pixel circuit according to the present embodiment. The pixel circuit has two features. The first feature is that a precharge acceleration circuit **8** is added to the pixel circuit shown in **FIG. 2**. The precharge acceleration circuit **8** is a circuit for outputting a predetermined voltage Vb. The voltage Vb is preferably in vicinities of the above-mentioned offset voltage (Vdd−Vth), but may be less than a voltage such that the driving transistor T**3** is turned on, (Vdd−Vth). The second feature is that the switching circuit **6** comprises a group of two switching transistors T**6** and T**7**. The switch-

ing transistor T**6** is provided between the data line X and the variable current source **4***a*, and is controlled by a first switching signal SWS**1**. Further, the switching transistor T**7** is provided between the data line X and the precharge acceleration circuit **8**, and is controlled by a second switching signal SWS**2**.

[0057] **FIG. 8** is a timing chart of operation of the pixel circuit shown in **FIG. 7**. A period t**0** to t**3** corresponding to one frame period (**1**F) is generally divided into a precharge acceleration period t**0** to t**0**', a precharge period t**0**' to t**1**, a data writing period t**1** to t**2** and a driving period t**2** to t**3**. The present embodiment is different from the first embodiment in that the precharge acceleration period t**0** to t**0**' is provided prior to the precharge period t**0**' to t**1**, and other processes are the same as those of the first embodiment.

[0058] First, in the precharge acceleration period t**0** to t**0**', the first scanning signal SEL**1** and the first switching signal SWS**1** are at L level, and then the switching transistors T**1**, T**2** and T**6** are turned off together. Accordingly, the data line X is electrically isolated from the node Ng and the variable current source **4***a*. In this state, the level of the second switching signal SWS**2** becomes H level, and then the switching transistor T**7** is turned on. Thus, the output voltage Vb from the precharge acceleration circuit **8** is supplied to the data line X, such that the data line X is precharged. If the precharge acceleration process is not provided, in the precharge period t**0** to t**1**, the precharge operation is performed with a current value close to a turn-off current of the driving transistor T**3**, and thus it is required for a certain degree of time to precharge. Therefore, in the present embodiment, prior to the precharge, the output voltage Vb is supplied to the data line X such that the driving transistor T**3** is turned on. Thus, the drain voltage of the driving transistor T**3** is set to a value close to the offset voltage (Vdd−Vth), whereby it is possible to assist and accelerate the operation of the subsequent precharge period t**0**' to t**1**.

[0059] The subsequent operation is the same as that of the first embodiment, and will be schematically described herein. In the precharge period t**0**' to t**1**, the precharge is performed by means of the diode-connected driving transistor T**3**, and the voltage Vg of the node Ng is set to the offset voltage (Vdd−Vth). In the data writing period t**1** to t**2**, data according to the product of the data current Idata and its supply time Δt is written, based on the offset voltage (Vdd−Vth) set in the previous precharge period t**0** to t**1**. And then, in the driving period t**2** to t**3**, the driving current Ioled which does not depend on the Vth of the driving transistor T**3** flows in the organic EL element OLED, whereby the organic EL element is emitted.

[0060] As described above, according to the present embodiment, like the respective embodiments described above, it is possible to suppress variation in the driving current Ioled depending on the Vth of the driving transistor T**3**. Further, in the present embodiment, prior to the precharge, the process for turning on the driving transistor T**3** is further provided. Thus, since the subsequent precharge can be completed in a relatively short time, it is possible to alleviate a time limit in a series of operation processes.

[0061] Moreover, the precharge acceleration technique described in the present embodiment can be applied similarly to the pixel circuits according to the fifth and sixth embodiments described below. However, in case of an application to the sixth embodiment, it is preferable to set the output voltage Vg of the precharge acceleration circuit **8** in vicinities of the offset voltage (V**1**+Vth).

Fourth Embodiment

[0062] The present embodiment is to implement the operation similar to the first embodiment, without providing the switching circuit **6** shown in **FIG. 1**. **FIG. 9** is a diagram of a pixel circuit according to the present embodiment. This configuration example has a feature that the switching transistor T**1** and T**2** in the pixel **2** are controlled the respective scanning signals SEL**1***a* and SEL**1***b*, instead of using the switching transistor T**6** shown in **FIG. 2**. Moreover, other elements are the same as those of the first embodiment, and thus the descriptions of like elements will be omitted.

[0063] **FIG. 10** is a timing chart of operation of the pixel circuit shown in **FIG. 9**. A period t**0**-t**3** corresponding to one frame period (**1**F) is generally divided into a precharge period t**0**-t**1**, a data writing period t**1**-t**2**, and a driving period t**2**-t**3**. The present embodiment is different from the first embodiment in that an ending timing t**1** of the precharge (in other words, a starting timing of the data writing) is defined by a rising of the scanning signal SEL**1***b*.

[0064] First, in the precharge period t**0** to t**1**, since the level of the scanning signal SEL**1***a* is H level and the switching transistor T**2** is turned on, the driving transistor T**3** is diode-connected. However, in this period t**0** to t**1**, since the level of the scanning signal SEL**1***b* is L level and the switching transistor T**1** is turned off, the node Ng is left to be electrically isolated from the variable current source **4***a*. As a result, until the node Ng reaches the offset voltage (Vdd−Vth), the precharge of the capacitor C**1** is performed. In the subsequent data writing period t**1** to t**2**, the level of the scanning signal SEL**1***b* rises to H level, the node Ng and the variable current source **4***a* are electrically connected, and thus the data writing based on the offset voltage (Vdd−Vth) is performed. Further, in the driving period t**2**-t**3**, the driving current Ioled generated by the driving transistor T**3** flows in the organic EL element OLED, whereby the organic EL element is emitted. Like the first embodiment, the driving current Ioled is determined by the product of the data current Idata and its supply time Δt, not depending on the Vin of the driving transistor T**3**.

[0065] According to the present embodiment, even when the switching circuit **6** is provided outside the pixel **2**, the precharge with the Vth compensated becomes possible. Thus, it is possible to suppress variation in the driving current Ioled depending on the Vth, and further it is possible to simplify the entire configuration of the electro-optical device.

Fifth Embodiment

[0066] The respective embodiments described above are not limited to the pixel circuit shown in **FIG. 2**, but may be widely applied to a current-programmed mode pixel circuit including a configuration example of a current mirror type described below. **FIG. 11** is a diagram of a pixel circuit according to the present embodiment. One pixel **2** comprises an organic EL element OLED, four transistors T**1** through T**4** and a capacitor C**1**. Moreover, in this configuration example, the driving transistor T**3** functions only as a

driving element, and the function of the programming element is implemented by a different programming transistor T4. Further, in the present embodiment, the n-channel type transistors T1 and T2 and the p-channel type transistors T3 and T4 are used, but it is just an example, and the channel types of the respective transistors T1 through T4 may be set differently from the above channel type combination.

[0067] The gate of the switching transistor T1 is connected to the scanning line to which the scanning signal SEL is supplied, and one terminal of the switching transistor T1 is connected to the data line X to which the data current Idata is supplied. The other terminal of the switching transistor T1 is commonly connected to one terminal of the switching transistor T2 and one terminal of the programming transistor T4. The gate of the switching transistor T2 is connected to the scanning line to which the scanning signal SEL is supplied, and the other terminal of the switching transistor T2 is connected to the node Ng. To the node Ng, the respective gates of a pair of the transistors T3 and T4 which constitute the current mirror and one electrode of the capacitor C1 are commonly connected. To one terminal of the driving transistor T3, the other terminal of the programming transistor T4 and the other electrode of the capacitor C1, the Vdd terminal is connected, to which the power source voltage Vdd is constantly supplied. To the other terminal of the driving transistor T3, the anode of the organic EL element OLED is connected, and to the cathode of the organic EL element OLED, the Vss terminal is connected, to which a reference voltage Vss is constantly supplied. The transistors T3 and T4 constitute a current mirror in which the gates of the transistors T3 and T4 are connected to each other. Accordingly, a current level of the data current Idata flowing in a channel of the programming transistor T4 is proportional to a current level of the driving current Ioled flowing in a channel of the driving transistor T3.

[0068] **FIG. 12** is a timing chart of operation of the pixel circuit shown in **FIG. 11**. A period t0-t3 corresponding to one frame period (1F) is generally divided into a precharge period t0-t1, a data writing period t1-t2 and a driving period t2-t3.

[0069] First, in the precharge period t0-t1, the precharge with the Vth compensated is performed. More specifically, the level of the scanning signal SEL becomes H level, and then the switching transistors T1 and T2 are turned on together. Thus, the data line X and one terminal (drain) of the programming transistor T4 are electrically connected, and further the programming transistor T4 is diode-connected in which its gate and its drain are electrically connected. In this period t0 to t1, since the level of the switching signal SWS is L level and the switching transistor T6 is turned off, the node Ng in the pixel 2 and the variable current source 4*a* are still left to be electrically isolated from each other. Thus, as shown in **FIG. 13**(*a*), the precharge of the capacitor C1 and the data line X is performed by the power source voltage Vdd of the Vdd terminal. By this precharge, the voltage of the node Vg, that is, the gate voltage Vg of the programming transistor T4 becomes the offset voltage (Vdd−Vth) depending on a threshold voltage Vth4 of the programming transistor T4.

[0070] Moreover, the electrical isolation of the node Ng and the variable current source 4*a* may be implemented by setting the variable current source 4*a* to a high impedance state, or may be implemented by controlling respectively the switching transistors T1 and T2. In case of adopting the above isolation techniques, the switching transistor T6 constituting the switching circuit 6 is not required. The same can be applied to the sixth embodiment described below.

[0071] Next, in the data writing period t1-t2, the data writing to the capacitor C1 is performed, based on the offset voltage (Vdd−Vth4) set in the previous precharge period t0-t1. In this period t1 to t2, since a level of the scanning signal SEL is the same as that of the precharge period t0-t1, the switching transistors T1 and T2 are left to be turned on. Further, in the timing t1, the level of the switching signal SWS rises to H level, the switching transistor T6 which is turned off is switched to be turned on. Thus, as shown in **FIG. 13**(*b*), the node Ng and the variable current source 4*a* are electrically connected to each other. As a result, a path of the data current Idata is formed, and the path is made in a sequence of the Vdd terminal, the channel of the programming transistor T4 and the variable current source 4*a*. As shown in the following equation 4, the voltage Vg of the node Ng is changed according to the product of the data current Idata and its supply time Δt, based on the previously set offset voltage (Vdd−Vth4). In the capacitor C1, charges corresponding to the voltage Vg are written as data. Moreover, in this period t1-t2, a path is formed in a sequence of the Vdd terminal, the driving transistor T3, the organic EL element OLED and the Vss terminal, and thus the driving current flows in the organic EL element OLED, whereby the organic EL element OLED starts to be emitted.

$$Vg=Vdd-Vth4-\Delta V$$

$$\Delta V=(Idata\cdot\Delta t)/C \qquad \text{(Equation 4)}$$

[0072] In the subsequent driving period t2-t3, the driving current Ioled corresponding to a channel current Isd of the driving transistor T3 is supplied to the organic EL element OLED, and thus grayscale level of the pixel 2 is defined. More specifically, levels of the scanning signal SEL and the switching signal SWS fall to L level, and then the switching transistors T1, T2 and T6 are turned off together. Thus, the node Ng is electrically isolated from the variable current source 4*a*. However, even after the electrical isolation, to the gate of the driving transistor T3, a voltage according to data stored in the capacitor C1 is continuously applied. As a result, through a path as shown in **FIG. 13**(*c*), the driving current Ioled flows. On an assumption that the driving transistor T3 operates in a saturation region, the driving current Ioled (the channel current Isd of the driving transistor T3) flowing in the organic EL element is calculated by the following equation 5 when a threshold voltage of the driving transistor T3 is Vth3.

$$Ioled=Isd=\tfrac{1}{2}\beta(Vsg-Vth3)^2 \qquad \text{(Equation 5)}$$

[0073] Here, if the voltage Vg calculated by the equation 4 is substituted for the gate voltage of the driving transistor T3, the equation 5 can be transformed to the following equation 6. Moreover, this equation transformation is on an assumption that the threshold voltage Vth3 of the driving transistor T3 and the threshold voltage Vth4 of the programming transistor T4 are the same (Vth3=Vth4=Vth). As regards the transistors T3 and T4 which are manufactured by the same process and arranged very closely to each other on the display unit 1, it is possible to set the electrical characteristics of the transistors T3 and T4 to be almost the same even in the actual product.

$$Ioled = 1/2\beta(Vs - Vg - Vth3)^2 \quad \text{(Equation 6)}$$
$$= 1/2\beta\{Vdd - (Vdd - Vth4 - \Delta V) - Vth3\}^2$$
$$= 1/2\beta \cdot \Delta V^2$$
$$= \beta/2(Idata \cdot \Delta t/C)^2$$

[0074] In the equation 6, it is important that the Vth**3** and Vth**4** are balanced each other during the equation transformation. This means that the driving current Ioled to be generated by the driving transistor T**3** does not depend on the Vth**3** and Vth**4**. The emitting brightness of the organic EL element OLED is principally determined by the driving current Ioled according to the product of the data current Idata and its supply time Δt, and thus grayscale level of the pixel **2** is set.

[0075] According to the present embodiment, like the respective embodiments described above, since it is possible to generate the driving current Ioled which does not depend on the Vth**3** and Vth**4**, it is possible to suppress variation in the driving current Ioled, and further it is possible to perform the precharge to be completed within the pixel **2**, even when an additional circuit for the precharge is provided outside the pixel **2**.

Sixth Embodiment

[0076] **FIG. 14** is a diagram of a pixel circuit according to the present embodiment. One pixel circuit comprises an organic EL element OLED, four n-channel type transistors T**1** through T**4** and a capacitor C**1**. In the present embodiment, since it is supposed that the TFT is made of amorphous silicon, the respective transistors are a n-channel type. Further, in this configuration example, the driving transistor T**3** functions as a programming element as well as a driving element primarily.

[0077] A gate of the switching transistor T**1** is connected to the scanning line to which the first scanning signal SEL**1** is supplied, and one terminal of the switching transistor T**1** is connected to one data line X to which the data current Idata is supplied. Further, the other terminal of the switching transistor T**1** is commonly connected to one terminal of the switching transistor T**2**, one terminal of the driving transistor T**3** and one terminal of the switching transistor T**4**. The gate of the switching transistor T**2** is connected to the scanning line to which the first scanning signal SEL**1** is supplied, and the other terminal of the switching transistor T**2** is connected to the node Ng. The node Ng is commonly connected to one electrode of the capacitor C**1** and the gate of the driving transistor T**3**. The other electrode of the capacitor C**1** is connected to a node Ns, and to the node Ns, the other terminal of the driving transistor T**3** and the anode of the organic EL element OLED are commonly connected. The cathode of the organic EL element OLED is connected to the Vss terminal to transistor T**4** is connected to the scanning line to which the second scanning signal SEL**2** is supplied, and the other terminal of the switching transistor T**4** is connected to the Vdd terminal to which the power source voltage Vdd is constantly supplied.

[0078] **FIG. 15** is a timing chart of operation of the pixel circuit shown in **FIG. 14**. A period t**0**-t**3** corresponding to one frame period (**1**F) generally divided into a precharge period t**0**-t**1**, a data writing period t**1**-t**2** and a driving period t**2**-t**3**.

[0079] First, in the precharge period t**0**-t**1**, the precharge with the Vth compensated is performed. More specifically, the level of the first scanning signal SEL**1** becomes H level, and then the switching transistors T**1** and T**2** are turned on together. Thus, the data line X and the node Ng are electrically connected, and the driving transistor T**3** is diode-connected in which its gate and its drain are electrically connected to each other. In this period t**0**-t**1**, since the level of the switching signal SWS is L level and the switching transistor T**6** is turned off, the node Ng in the pixel **2** and the variable current source **4***a* are still left to be electrically isolated from each other. Further, since the level of the second scanning signal SEL**2** is L level and the switching transistor T**4** is turned off, one terminal of the driving transistor T**3** and the Vdd terminal are electrically isolated from each other. Thus, as shown in **FIG. 16**(*a*), the precharge of the capacitor C**1** and the data line X is performed. By this precharge, the voltage of the node Ns becomes V**1**, and the voltage Vg of the node Ng becomes an offset voltage (V**1**+Vth) depending on the Vth of the driving transistor T**3**. Moreover, a specified value of the V**1** is depending on a leak current of the organic EL element OLED.

[0080] Next, in the data writing period t**1**-t**2**, the data writing to the capacitor C**1** is performed, based on the offset voltage (V**1**+Vth) set in the previous precharge period t**0**-t**1**. In this period t**1**-t**2**, since the levels of the scanning signals SELL and SEL**2** are the same as those in the precharge period t**0**-t**1**, the switching transistors T**1** and T**2** are left to be turned on and the switching transistor T**4** is left to be turned off. Further, in the timing t**1**, the level of the switching signal SWS rises to H level, and then the switching transistor T**6** which is turned off is switched to be turned on. Thus, as shown in **FIG. 16**(*b*), the node Ng and the variable current source **4***a* are electrically connected to each other. As a result, a path of the data current Idata is formed, and the path is made in a sequence of the variable current source **4***a*, the channel of the driving transistor T**3**, the organic EL element OLED and Vdd terminal. As shown in the following equation 7, the voltage Vg of the node Ng is changed by the product of the data current Idata and its supply time Δt, based on the previously set offset voltage (V**1**+Vth).

$$Vg = V1 + Vth1 + \Delta V$$
$$\Delta V = (Idata \cdot \Delta t)/C \quad \text{(Equation 7)}$$

[0081] Further, as shown in the equation 8, the voltage Vs of the node Ns is changed by ΔV' based on the voltage V**1** previously set. The ΔV' is a voltage depending on characteristics of the organic EL element OLED (V-I characteristic and Idata characteristic).

$$Vs = V1 + \Delta V' \quad \text{(Equation 8)}$$

[0082] In the subsequent driving period t**2**-t**3**, the driving current Ioled corresponding to the channel current Isd of the driving transistor T**3** is supplied to the organic EL element OLED, whereby the organic EL element is emitted. More specifically, levels of the first scanning signal SEL**1** and the switching signal SWS fall to L level, and then the switching transistor T**1**, T**2** and T**6** are turned off together. Thus, the node Ng is electrically isolated from the variable current source **4***a*. However, even after the electrical isolation, to the gate of the driving transistor T**3**, a voltage according to data

stored in the capacitor **C1** is continuously applied. Further, in synchronization with a falling of the first scanning signal SEL**1**, the level of the second scanning signal SEL**2** rises to H level, and then the switching transistor T**4** is turned on. Thus, to one terminal of the driving transistor T**3**, the power source voltage Vdd is supplied via the vdd terminal. Therefore, through a path as shown in **FIG. 16**(*c*), the driving current Ioled flows. On an assumption that the driving transistor T**3** operates in a saturation region, the driving current Ioled (the channel current Isd of the driving transistor T**3**) flowing in the organic EL element OLED is calculated by the following equation 9.

$$Ioled=Isd=\tfrac{1}{2}\beta(Vgs-Vth)^2 \quad \text{(Equation 9)}$$

[0083] Here, if the voltage Vg calculated by the equation 7 and the voltage Vs calculated by the equation 8 are substituted for the gate voltage of the driving transistor T**3**, the equation 9 can be transformed to the following equation 10.

$$\begin{aligned}\text{Ioled} &= 1/2\beta(Vg-Vs-Vth)^2 \quad \text{(Equation 10)}\\ &= 1/2\beta\{(V1+Vth+\Delta V)-(V1+\Delta V')-Vth\}^2\\ &= 1/2\beta(\Delta V-\Delta V')^2\\ &= \beta/2(Idata\cdot\Delta t/C-\Delta V')^2\end{aligned}$$

[0084] In the equation 10, it is important that the Vths are balanced each other during the equation transformation. This means that the driving current Ioled to be generated by the driving transistor T**3** does not depend on the Vth. The emitting brightness of the organic EL element OLED is principally determined by the driving current Ioled according to the product of the data current Idata and its supply time Δt, and thus grayscale level of the pixel **2** is set.

[0085] According to the present embodiment, like the respective embodiments, since it is possible to generate the driving current Ioled which does not depend on the Vth, it is possible to suppress variation in the driving current Ioled. At the same time, even when an additional circuit for the precharge is provided outside the pixel **2**, it is possible to perform the precharge to be completed with the pixel **2**.

[0086] Moreover, in the respective embodiments described above, the configuration example of the pixel circuit in which the transistor functioning as the programming element is selectively diode-connected by the control of the switching transistor is described. However, the present invention can also be applied to a pixel circuit in which the transistor functioning as the programming element is normally diode-connected.

[0087] Further, in the respective embodiments described above, the example in which the organic EL element is used for the electro-optical device is described. However, the present invention is not limited to the example, but the present invention can be widely applied to an electro-optical device in which the brightness is set according to the driving current (an inorganic LED display device, a field emission display device or the like), or an electro-optical device which exhibits transmittance and reflectance according to the driving current (an electrochromic display device, an electrophoretic display device or the like).

[0088] In addition, the electro-optical devices according to the respective embodiments can be mounted on various electronic apparatuses, for example, including a television, a projector, a personal digital assistant, a mobile type computer, a personal computer. If the above-mentioned electro-optical device is mounted on the respective electronic apparatuses, it is possible to increase the product value of the electronic apparatuses still more, and further it is possible to improve the product solicitation power in the market.

What is claimed is:

1. A method of driving a pixel circuit, comprising:

a first step of setting a gate voltage of a diode-connected first transistor to an offset voltage according to a threshold voltage of the first transistor, in a state in which a variable current source variably generating a data current is electrically isolated from the first transistor;

a second step of writing, in a capacitor connected to a gate of the diode-connected first transistor, data set based on the offset voltage and according to a product of the data current supplied from the variable current source via data lines and a supply time thereof, in a state in which the variable current source and the first transistor are electrically connected to each other; and

a third step of generating a driving current according to the data stored in the capacitor by a second transistor whose gate is connected to the capacitor to set the brightness of an electro-optical device.

2. The method of driving a pixel circuit according to claim 1, wherein a transistor rolls as both the first transistor and the second transistor.

3. The method of driving a pixel circuit according to claim 1, wherein the first transistor and the second transistor constitute a current mirror.

4. The method of driving a pixel circuit according to claim 1, wherein

the first step comprises a step of turning off switching elements provided between the variable current source and the first transistor, and

the second step comprises a step of turning on the switching elements.

5. The method of driving a pixel circuit according to claim 1, further comprising:

a fourth step of regulating the offset voltage set in the first step, by variably controlling the terminal voltage of a capacitor that another terminal is coupled to the data lines.

6. The method of driving a pixel circuit according to claim 5, wherein in the fourth step, the amount of change of the terminal voltage of a capacitor is set according to a grayscale level to be displayed.

7. The method of driving a pixel circuit according to claim 1, further comprising:

prior to setting the offset voltage in the first step, a fifth step of supplying, to the data lines, a predetermined voltage having a voltage level that turns on the first transistor.

8. A pixel circuit comprising:

a first transistor, normally or selectively diode-connected under the control of a switching transistor, for generating data according to a data current supplied from a variable current source via a data line;

a capacitor connected to a gate of the first transistor, in which data generated by the first transistor is written;

a second transistor, whose gate is connected to the capacitor, for generating a driving current according to the data stored in the capacitor; and

an electro-optical element in which the brightness is set according to the driving current generated by the second transistor,

wherein in a state which the first transistor is electrically isolated from the variable current source, the first transistor

sets its gate voltage to an offset voltage according to its threshold voltage, and

wherein in a state which the first transistor is electrically connected to the variable current source, the first transistor

writes, in the capacitor, data set based on the offset voltage and according to a product of the data current supplied from the variable current source and a supply-time thereof.

9. The pixel circuit according to claim 8, wherein a transistor rolls as both the first transistor and the second transistor.

10. The pixel circuit according to claim 9, wherein the first transistor and the second transistor constitute a current mirror.

11. The pixel circuit according to claim 8, further comprising:

a switching circuit for electrically isolating the variable current source from the data lines for a period during which the gate voltage is set to the offset voltage, and electrically connecting the variable current source to the data lines for a period during which the data is written in the capacitor.

12. The pixel circuit according to claim 8, further comprising:

a precharge regulation circuit that regulate the offset voltage by variably controlling the terminal voltage of a capacitor that another terminal is coupled to the data lines.

13. The pixel circuit according to claim 12, wherein the precharge regulation circuit controls the amount of change of the terminal voltage of a capacitor according to a grayscale level to be displayed.

14. The pixel circuit according to claim 8, further comprising:

a precharge acceleration circuit for supplying, to the data lines, a predetermined voltage having a voltage level that turns on the first transistor, prior to a period during which the gate voltage is set to the offset voltage.

15. An electronic apparatus comprising an electro-optical device comprising the pixel circuit as claimed in claim 8.

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